SPECIFICATION

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[*METHOD OF PREVENTING LEAKAGE CURRENT OF A METAL-OXIDE SEMICONDUCTOR TRANSISTOR*]

Cross Reference To Related Applications

This is a continuation-in-part of U.S. Application No. 09/683,691, filed February 4, 2002, and which is included herein by reference.

Background of Invention

[0001] 1.Field of the Invention

[0002] The present invention relates to a method of forming a metal-oxide semiconductor (MOS) transistor on a substrate, and more specifically, to a method of forming a MOS transistor with a step source/drain extension to reduce leakage current caused by a self-aligned silicide (salicide) process.

[0003] 2.Description of the Prior Art

[0004] Metal oxide semiconductor (MOS) transistors are in wide use in many electric devices. A MOS transistor has four terminals: the source, the drain, the gate, and the substrate. When a gate voltage greater than a threshold voltage of a MOS transistor is applied to the gate, a channel forms between the source and the drain due to strong inversion. Consequently, the electrical performance of the gate is an important issue in the semiconductor industry.

[0005] Please refer to Fig.1 of a schematic view of a MOS transistor according to the prior art. As shown in Fig.1, a MOS transistor 10 comprises a substrate 12, a gate oxide

layer 14 located on the substrate 12, a gate 16 located on the gate oxide layer 14, a lightly doped drain (LDD) 24 either in portions of the substrate 12 adjacent to either side of the gate 16, a pair of spacers 20 positioned on both sides of the gate 16, and a source/drain 18a/18b formed in portions of the substrate 12 adjacent to either side of the spacer 20. In addition, contact plugs (not shown), which are located upon the gate 16, the source 18a, and the drain 18b, electrically connect the MOS transistor 10 and any other metal conductors (not shown). In general, a silicide layer 22 is formed on the gate 16, the source 18a and the drain 18b in order to reduce the contact resistance of each silicon surface. Then, contact plugs are formed on the silicide layer 22.

[0006] The LDD 24 has a high resistivity and is thus replaced by an ultra shallow junction (USJ, not shown in Fig.1) as the manufacturing line width is less than 0.18 microns. Due to an increase in the complexity of integrated circuits, sizes of MOS transistors are reduced to increase the amounts of MOS transistors per unit area. However, the shallower the junction depth of the ultra shallow junction, the smaller the distance between a bottom of the source 18a/drain 18b and a bottom of the silicide layer 22. As a result, shrinking the sizes of MOS transistors causes the diffusion of metal atoms in the silicide layer 22 into the substrate 12 and increases the leakage current of the MOS transistor 10. In addition, as the width of the gate 16 reduced due to the reduction of the size of the MOS transistor 10, the correspondingly decreased distance between the two ultra shallow junctions on opposite sides of the gate 16 frequently lead to a punch through phenomenon of the MOS transistor 10. The performance of the MOS transistor 10 is therefore reduced.

Summary of Invention

[0007] It is therefore a primary object of the present invention to provide a method of fabricating a metal-oxide semiconductor (MOS) transistor.

[0008] It is another object of the present invention to provide a method of preventing the leakage current in an ultra shallow junction of a source/drain extension of the MOS transistor.

[0009]

According to the claimed invention, a gate oxide layer and a gate are sequentially

formed on a silicon substrate. By performing a first ion implantation process, the source/drain extension is formed in the silicon substrate. A liner layer is then formed to cover the silicon substrate, and a dielectric layer and a sacrificial layer are sequentially formed on the liner layer thereafter. By performing a first etching process, an arc-shaped spacer is formed on either side of the gate, and portions of the dielectric layer and the sacrificial layer atop the gate are removed. A L-shaped spacer is then formed on either side of the gate by performing a second etching process to remove portions of the sacrificial layer within the arc-shaped spacer. By performing a third etching process, portions of the liner layer not covered by the L-shaped spacer are removed. By performing a second ion implantation process, a step source/drain extension and a source/drain are simultaneously formed in the silicon substrate, wherein the source/drain extension, the step source/drain extension and the source/drain are in a gradient profile. Finally, a self-aligned silicide (salicide) process is performed to form a silicide layer on the gate and on portions of the silicon substrate surface above the source/drain.

[0010] It is an advantage of the present invention against the prior art that a plurality of ion implantation processes is performed to form the source/drain extension, the step source/drain extension and the source/drain in the gradient profile, increasing the distance between a bottom of the source/drain and a bottom of the silicide layer. The leakage current in the ultra shallow junction of the source/drain extension of the MOS transistor is thus prevented. In addition, a punch through phenomenon of the MOS transistor as described in the prior art is prevented as well. Therefore, as sizes of MOS transistors are reduced to increase the amounts of MOS transistors per unit area due to an increase in the complexity of integrated circuits, the method of fabricating the MOS transistor provided in the present invention can assure the performance of the MOS transistor, making the product more competitive.

[0011] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

Brief Description of Drawings

[0012] Fig.1 is a schematic view of a MOS transistor according to the prior art.

[0013] Fig.2 to Fig.8 are schematic views of fabricating a metal-oxide semiconductor (MOS) transistor according to the present invention.

Detailed Description

[0014] Please refer to Fig.2 to Fig.8 of schematic views of fabricating a metal-oxide semiconductor (MOS) transistor according to the present invention. As shown in Fig.2, a silicon substrate 40 is provided with a gate oxide layer 42 and a gate 44 sequentially formed on the silicon substrate 40. At the beginning of the method, a first ion implantation process is performed to form a source/drain extension (SDE) 46 in the silicon substrate 40, and a liner layer 48, comprising silicon oxide, is then formed to cover the silicon substrate 40. In the preferred embodiment of the present invention, the source/drain extension 46 is doped with either arsenic (As) atoms or phosphorus (P) atoms. Alternatively, the source/drain extension 46 is doped with either one of boron difluoride (BF_2^+) ions, boron (B) atoms or indium (In) atoms. In another embodiment of the present invention, the gate 44 further comprises an offset spacer (not shown in Fig.2 to Fig.8) on either side of the gate 44.

[0015] As shown in Fig.3, a dielectric layer 50, comprising nitride, and a sacrificial layer 52, comprising polysilicon, are then sequentially formed on the liner layer 48. As shown in Fig.4, by utilizing the liner layer 48 as a stop layer, a first etching process is performed to form an arc-shaped spacer 54 on either side of the gate 44 and to remove portions of the dielectric layer 50 and the sacrificial layer 52 atop the gate 44.

[0016] As shown in Fig.5, by utilizing the dielectric layer as a stop layer, a second etching process is performed to remove portions of the sacrificial layer 52 within the arc-shaped spacer 54, forming a L-shaped spacer 56 on either side of the gate 44. A third etching process is then performed to remove portions of the liner layer 48 not covered by the L-shaped spacer 56, exposing a top surface of the gate 44 and portions of the source/drain extension 46.

[0017] As shown in Fig.6, using either arsenic atoms or phosphorus atoms as dopants, a second ion implantation process is then performed to simultaneously form a step source/drain extension 58 and a source/drain 60 in the silicon substrate 40. In another embodiment of the present invention, the step source/drain extension 58 and

the source/drain 60 are doped with either one of boron difluoride ions, boron atoms or indium atoms. Wherein the depth and the width of the step source/drain extension 58 are respectively determined by the thickness of the dielectric layer 50 and the width of the L-shaped spacer 56, and the source/drain extension 48, the step source/drain extension 58 and the source/drain 60 are in a gradient profile.

[0018] As shown in Fig.7, a metal layer 62 is then formed to cover the silicon substrate 40. In the preferred embodiment of the present invention, the metal layer 62 is composed of cobalt (Co). As shown in Fig.8, a first rapid thermal process (RTP) is then performed, activating the reaction of the metal layer 62 with the silicon substrate 40. A wet etching process is then performed to remove unreacted portions of the metal layer 62 on the surface of the silicon substrate 40. Finally, a second RTP is performed to form a silicide layer 64 on the gate 44 and on portions of the surface of the silicon substrate 40 above the source/drain 60. The method of forming the silicide layer 64 comprising the steps described in this paragraph is called a self-aligned silicide (salicide) process.

[0019] As previously mentioned, due to an increase in the complexity of integrated circuits, sizes of MOS transistors are reduced to increase the amounts of MOS transistors per unit area. Therefore, the depth of the source/drain extension 46 decreases and an ultra shallow junction of the source/drain extension 46 is thus formed. In comparison with the prior art, the method of fabricating a MOS transistor provided in the present invention utilized a plurality of ion implantation processes to form the source/drain extension 46, the step source/drain extension 58 and the source/drain 60 in the gradient profile, increasing the distance between a bottom of the source/drain 60 and a bottom of the silicide layer 64. The leakage current in the ultra shallow junction of the source/drain extension 46 of the MOS transistor is thus prevented. In addition, a punch through phenomenon of the MOS transistor as described in the prior art is prevented as well. Therefore, as sizes of MOS transistors are reduced to increase the amounts of MOS transistors per unit area due to an increase in the complexity of integrated circuits, the method of fabricating the MOS transistor provided in the present invention can assure the performance of the MOS transistor, making the product more competitive.

[0020] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bound of the appended claims.